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Implementation of a parallel SAD based wavefront sensor architecture on FPGA

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Abstract— Wavefront aberration caused by turbulent or rapidly changing media can considerably degrade the performance of an imaging system. Adaptive optics can dynamically compensate these wavefront distortions and so provide corrected imaging. We developed an affordable adaptive optic system which combines CMOS sensor and LCOS display technology with the FPGA devices parallel computing capabilities. High speed and accurate wavefront sensor is fundamental part of any adaptive optic system. In this paper, an efficient FPGA implementation of the Sum of Absolute Differences (SAD) algorithm is introduced which accomplish correlation based wavefront sensing. This architecture was implemented on a Spartan-3 FPGA and capable to measure the incoming wavefront at the speed of sensor data acquisition speed.

Keywords- FPGA, wavefront sensor, SAD

I. INTRODUCTION

Rapidly changing, turbulent media cause wavefront distortions, which results in random phase aberration to the imaging system. Wavefront sensors can measure these wavefront distortions and within an Adaptive Optic (AO) system they can be dynamically compensated using some actuator device [1, 2]. This way AO system provides an aberration corrected imaging. Adaptive optic devices can be applied not only in astronomic telescopes where it has to cope primarily with the atmospheric turbulences, but also in other diverse fields from ophthalmology to laser welding, or to telecommunication.

We have developed a simple, affordable adaptive optic system, which combines high speed CMOS sensor, Liquid Crystal On Silicon (LCOS) display, and Field Programmable

Gate Arrays (FPGA) technology. Although, our project primarily aims a special solar telescopic application, but introduction of an affordable adaptive optic system can open new scopes.

Here we apply the most frequently used Hartmann-Shack (HS) sensor. In a HS sensor the image of the incoming pupil is projected on a lenslet and each lens of the array forms a miniature image of the source object where an area scan sensor measures it. Shift of these sub-images from the central position is proportional to the corresponding sub aperture local wavefront slopes (wavefront is regarded locally tilted but flat).

For point source objects a simple quad cell sensor can be applied, but for extended objects these shifts can be measured by its correlation to a reference sub aperture image. Assembling all these local slopes the wavefront of the whole pupil can be approximated. Although correlation based HS sensors are more efficient than quad cells from signal to noise point of view [3], but requires considerably more computing resources. Even for first order aberration compensation (tip-tilt) high speed correlation trackers are used to be applied [4].

In conventional applications the wavefront local slopes has to be measured using numerous, relatively large resolution sub apertures at a very high rate (turbulent media). This way high resolution, real time correlation based wavefront sensor is required [5]. Some parallel processing devices can fulfill these requirements. Although, other technologies [6] can also grant the required computation power, application of FPGA technology is considered here. As the control of the sensor and actuator usually requires a programmable logic device so it seems to be advantageous to apply them to fulfill the required

computation tasks also. This way communication bottlenecks can be avoided and higher speed can be granted for a closed loop system. Several FPGA based wavefront sensor and AO system architecture was introduced so far [7, 8, 9].

In our AO system, according to the measured and digitally reconstructed wavefront distortions a built in LCOS device displays the corrections. Distortion of the incoming wavefront is measured using a HS wavefront sensor.

Due to the FPGA device limitations and special constraint of the HS sensor a Sum of Absolute Difference (SAD) method is applied to implement the required correlation like processing. Due to the motion image compression FPGA implementation claims several efficient SAD algorithms has been emerged [10].

The best matching position of two pictures can be determined by the SAD algorithm. First the SAD values of the picture are calculated, and then the minimum of them is determined. Using this method the displacement of all sub aperture images is determined with respect to a reference image. A high contrast central sub aperture image is chosen as proper reference image. SAD values are computed according to the next equation.

$$SAD_{k,l} = \sum_i^S \sum_j^S |P_{i,j} - R_{i+k,j+l}|, k,l < A, \quad (1)$$

where S is the size of the sub aperture, A is the size of the SAD value array, P is the sub aperture pixel, and R is the reference pixel accordingly. The size of the reference image is the sum of the size of the sub aperture and the SAD value array minus one. Practically the size of the SAD value array is smaller than the size of the sub aperture.

In this paper a new highly parallel FPGA based SAD implementation will be introduced which takes into account the special requirements of the correlation based wavefront sensor.

II. THE FPGA BASED ADAPTIVE OPTIC SYSTEM

Our FPGA based adaptive optic system contains three main components. The first part is the 1280×1024 pixels resolution Micron MT9M413 CMOS image sensor which is able to acquire 500 full image frames per second. This sensor is extended with an array of micro lenses, called lenslet (32×32 each of them cover 16×16 pixel sized sub aperture on the sensor surface). The second part is the Philips DD720 Liquid Crystal On Silicon (LCOS) display sold by HoloEye, its resolution is 1280×768 pixels with 20 μm pixel sizes and up to 540 full image frames can be displayed within a second. Using this device amplitude or phase modulation can be carried out using appropriate wave plates and polarizers. The on board Xilinx Spartan-3 XC3S4000 FPGA is responsible for the control of the overall system and the calculation of the correction data. The density of this FPGA is 4 million system gates. It is equipped with 96 18Kb BlockRAM and 18×18bit multipliers.

III. THE IMPLEMENTED ARCHITECTURE ON FPGA

Our primary goal is to implement a high speed and highly parallel architecture on the FPGA to determine the displacement of the sub apertures in order to calculate the wavefront distortions. The block diagram of the architecture implemented on FPGA is shown in Fig. 1.

The Micron CMOS sensor is controlled and image data is received by CMOS controller. The LCOS unit is responsible for the computation of the correction terms and sending them to the LCOS display. The sub-pixel resolution motion vectors are determined by the Xilinx MicroBlaze soft core processor. The reference image and the coordinates of the sub apertures are defined by the host computer via the USB controller.

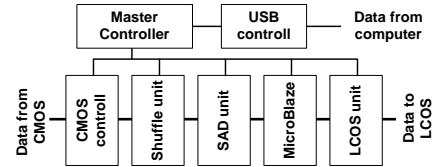


Figure 1. The implemented architecture of the overall system on FPGA

A. The Shuffle unit

The Shuffle unit is responsible for serializing the pixels required for the calculation of the SAD values. During the image capturing only pixels of the sub apertures are used, therefore SAD values should be computed (to determine the wavefront) in these areas. The relevant pixels in respect with the coordinates of the sub apertures are defined by the host computer. Selection and serialization of the incoming pixels from the CMOS sensor is performed by the Shuffle unit.

B. The SAD unit

The main building blocks of the SAD unit are the Reference Register unit, the Absolute Differences unit, the SAD Controller unit and the Minimum Finder unit as can be seen in Fig. 2. In addition to these elements, the SAD unit also contains an accumulator register array to sum the computed Absolute Difference (AD) values and BlockRAMs to store the partial SAD results.

The SAD unit is designed to compute (1) on the sub apertures of the input image in real-time. Image data is sent by the CMOS sensor in a row-wise order therefore $S \times S$ pixel should be stored to carry out the computation of the SAD values. Additionally there are several sub apertures in the row which further increases the memory requirements. This is impractical in the case of large sub apertures. Instead of storing the sub aperture windows, computation of the SAD values is rearranged to match the incoming dataflow and all partial SAD values are computed in parallel. For example when the first pixel $P_{0,0}$ is arrived, the first term of (1) - $AD_{k,l,0,0} = |P_{0,0} - R_{k+i,l+j}|$ - is computed for all possible k,l values. When partial results using the first row of the sub aperture is computed the SAD values are stored in a temporary buffer and computation with the next sub aperture is started. Storing these partial SAD values requires less memory than double buffering the incoming sub aperture data.

The Reference Register stores the reference values and generates the appropriate reference window for the actual pixel of the sub aperture. The $A \times A$ pixel sized reference window is moving left to right during the computation. Architecture of the Reference Register unit is shown in Fig. 3 in case of the 5×5 pixel sized reference picture.

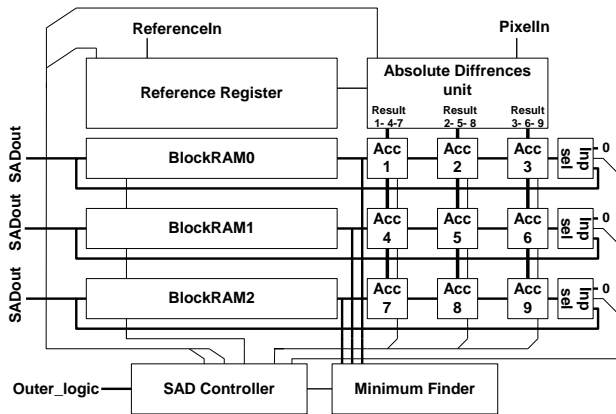


Figure 2. The architecture of the SAD unit in case of 3×3 pixel sized sub aperture

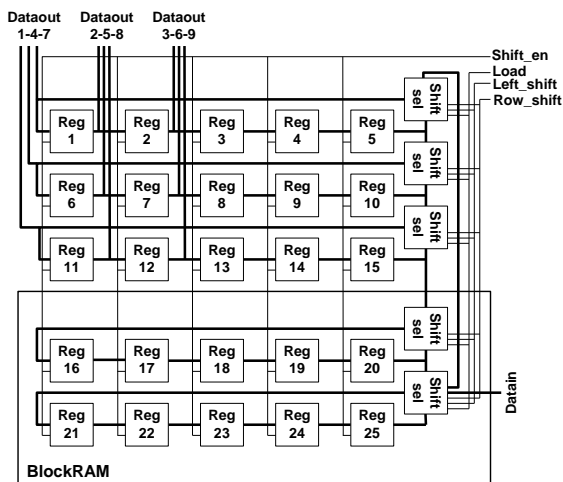


Figure 3. The architecture of the Reference Register unit in 5×5 pixel sized case

To make implementation simpler and to utilize the shift register resources in the FPGA the reference window is fixed and the reference values are shifted in our system. The required 9 reference values in the example are always placed on the upper left side of the reference array in a 3×3 sized window.

Thus the Reference Register unit has three operation modes: the load, the left shift and the row shift mode. In the load mode the reference values are loaded into the bottom right register (Reg25) and shifted left in the register chain in a pixel wise manner. In the left shift mode values in the registers are shifted circularly in the same row. Finally the row shift mode is very similar to the load mode except in the case of the lower right register (Reg25) which is loaded with the contents of the upper left register (Reg1).

The Absolute Differences unit is responsible for calculating the absolute differences between the reference and the input image. This unit is built up from an array of processing elements. The number of processing elements is defined by the size of the sub aperture. Thus all the AD values can be calculated in parallel. The structure of one processing element is shown in Fig. 4.

The Minimum Finder unit defines the smallest SAD value and the 4-connected neighborhood of it, and the SAD Controller unit controls the operation of the SAD unit.

According to the wavefront sensing algorithm, where 8×8 to 32×32 pixel sized sub apertures are required, the size of the reference image, which defines the size of the SAD value array, the size and number of the sub apertures is configurable in the VHDL description of the unit.

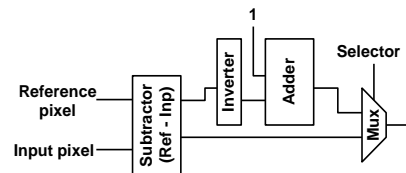


Figure 4. The structure of a processing element in the Absolute Differences unit

Additionally, several SAD units can work parallel by slicing the input image and using more Shuffle units.

IV. RESULTS

An FPGA based adaptive optic system was constructed and the architecture of the wavefront sensor system was implemented on a Spartan-3 XC3S4000 FPGA using VHDL language. Maximal size of the sub aperture is limited by the area requirement of SAD units on the FPGA.

The number of applicable sub apertures is bounded by the row length of the CMOS sensor. The 18Kb BlockRAMs used in the SAD unit is large enough to store the entire row of computed SAD values in our case. The size of the sub apertures is important since it defines the required number of BlockRAMs and other logical resources on the FPGA. The performance of the SAD unit is investigated in case of different sub aperture and reference image sizes. Static timing analysis of the placed and routed designs is shown that the speed of the SAD unit can reach the 120 MHz operating frequency in all cases. The Flip-Flop resource utilization of the implemented SAD unit on the Spartan-3 XC3S4000 FPGA can be seen in Fig. 5.

The Flip-Flop resource requirement of the SAD unit is increasing quadratically according to the size of the sub apertures, but does not depend on the size of the SAD value array. The same behavior can be obtained in case of the 4-input LUT and BlockRAM resource requirement of the SAD unit. If the size of the sub aperture is increased to the 32×32 pixel resolution, the resources in the Spartan-3 XC3S4000 FPGA will not be enough. To handle 32×32 pixel sized or larger sub apertures denser and higher performance FPGAs (Virtex-4) should be used. To achieve even faster performance

several SAD units can be used in parallel. The number of realizable SAD units is determined by BlockRAM resources on the FPGA in case of SAD value arrays smaller than 12×12. For larger SAD value arrays the bottleneck is the number of available Flip-Flops on the device.

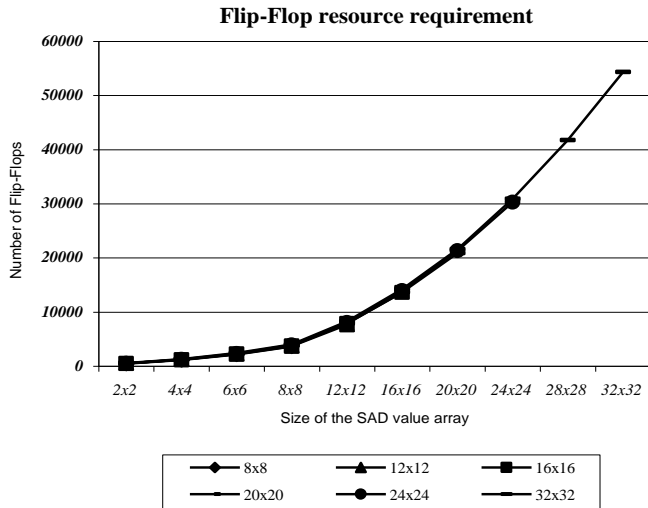


Figure 5. The Flip-Flop resource requirement of the SAD unit in case of different size of sub apertures

The SAD unit requires different number of clock cycles to calculate the SAD values according to the size of the sub apertures as shown on Table I. in case of maximal SAD value array size. Thus the number of real time manageable sub apertures is different. One SAD unit running on 120MHz clock frequency can handle 2172 8×8 pixel resolution sub apertures on each frame of the CMOS sensor in real-time. However this is only 40.44% of the surface of the CMOS sensor, but requires only 9.4% of the FPGA resources. Therefore using three SAD units on the Spartan-3 FPGA the whole surface of the CMOS sensor can be processed in real time. Using 24×24 pixel sized sub apertures 228 sub apertures can be handled in real time. This makes it possible to process the 40.13% of the entire surface of the CMOS sensor. Using higher performance Virtex-4 LX100 FPGA also the whole surface of the CMOS sensor can be processed in real time using 24×24 pixel sized sub apertures.

TABLE I. THE TEST RESULTS OF THE SAD UNIT

Sub aperture size in pixels	Required number of clock cycles	Maximum number of sub apertures/frame	Percentage of the CMOS surface
8x8	225	2172	40.44 %
12x12	529	941	41.38%
16x16	961	522	40.81 %
20x20	1521	331	40.42%
24x24	2209	228	40.13%
32x32*	3969	243	76.04%

* in case of Virtex-4 LX100 FPGA

Our results are compared to a correlation based wavefront sensor system described in [11]. This system is implemented on Xilinx Virtex-4 SX35-10. The processing core is operating on 100MHz clock frequency, so for the better comparison

results the clock frequency of our SAD unit is also decreased to 100MHz. The result of the comparison of the SAD unit implemented on Spartan-3 XC3S4000 and the correlation based system is shown on Table II.

TABLE II. THE COMPARISON OF THE DIFFERENT IMPLEMENTATIONS

	CMOS area: 256×256 Sub aperture: 8×8 (in pixels)		CMOS area: 512×512 Sub aperture: 16×16 (in pixels)	
	Correlation	SAD	Correlation	SAD
Slices	5431	3435	9932	10186
LUTs	10161	2769	18607	12093
Flip-flops	2096	3615	5981	13615
Time	2890 μs	1262 μs	18100 μs	5227 μs
AT	15.69	4.33	179.76	53.24

The results show that the Area*Time (AT) parameter of our SAD based wavefront sensor system is better than correlation based system described in [11]. In case of 8×8 pixel sized sub apertures, the AT parameter of our SAD unit is 27% better than the correlation based system. This ratio is increasing when larger sub apertures are used. In 16×16 pixel sized case, performance difference is 30% between the two types of implementation. Performance advantage of our system can be further increased by using more SAD units additionally its operating frequency is also higher (especially in case of Virtex-4).

V. CONCLUSION

A new wavefront sensor system based on the high speed and highly parallel SAD calculation unit was implemented on the Spartan-3 FPGA. This system can be used with wide range of applicable lenslets, because it is fully configurable with respect to the size and the number of sub apertures and reference images. Performance of the system was tested on differently sized sub apertures. The results show that the resource requirement of the SAD calculation unit is increasing quadratically according to the size of the sub apertures, but not depends on the size of the SAD value array. Considering 8×8 pixel sized sub apertures the entire surface of the CMOS sensor can be processed in real time using three SAD units on the Spartan-3 XC3S4000 FPGA. In case of higher resolution sub apertures, the real time processable CMOS surface is reduced. But using higher performance FPGAs (Virtex-4) also makes it possible to handle the whole area of the CMOS sensor in real time. Performance advantage of our system compared to correlation based wavefront sensor architectures is 27% in 8×8 pixel sized case. This difference is further increased when larger sub apertures are used. The cost of the proposed system is a fraction of the cost of the other adaptive optic systems.

REFERENCES

- [1] Dayton, D., Goglewski, J., Restaino, S., Martin, J., Philips, J., Hartman, M., Kervin, P., Snodgrass, J., Browne, S., Heimann, N., Shilko, M., Pohle, R., Carrion, B., Smith, C. and Thiel, D., "Demonstration of new technology MEMS and liquid crystal adaptive optics on bright astronomical objects and satellites," Opt. Express 10, 1508-1519 (2002).
- [2] Richards, K., Rimmel, T., Hill, R., Chen, J., "High speed low latency solar adaptive optics camera", Proc. SPIE, 5171, 316-325 (2004).
- [3] Poyneer, L.A., Palmer, D.W., LaFortune, K. N., Bauman, B., "Experimental results for correlation-based wavefront sensing,"

Advanced Wavefront Control: Methods, Devices, and Applications III. Proc. SPIE, Volume 5894, pp. 207-220 (2005).

- [4] Chang-Hui Rao, Wen-Han Jiang, Cheng Fang, Ning Ling, Wei-Chao Zhou, Ming-De Ding, Xue-Jun Zhang, Dong-Hong Chen, Mei Li, Xiu-Fa Gao and Tian Mi "A Tilt-correction Adaptive Optical System for the Solar Telescope of Nanjing University" Chin. J. Astron. Astrophys. Vol. 3 (2003), No. 6, 576–586
- [5] Serati, S., Xiaowei, X., Mughal, O., Linnenberger A., "High-resolution phase-only spatial light modulators with sub-millisecond response," Proc. SPIE, 5106, 138-145 (2003).
- [6] Rosa, F.L., Marichal-Hernandez, J.G., Rodríguez-Ramos, J.M., "Wavefront phase recovery using graphic processing units (GPUs)," Optics in Atmospheric Propagation and Adaptive Systems VII. Proc. SPIE, 5572, 262-272 (2004)
- [7] Saunter C.D., Love G.D., Johns, M., Holmes, "FPGA technology for high speed, low cost adaptive optics" J. in Proc. 5th International Workshop on Adaptive Optics in Industry and Medicine (2005).
- [8] Rodríguez-Ramos, L. F., Viera, T., Herrera, G., Gigante, J.V., Gago, F., Alonso, Á., "Testing FPGAs for real-time control of adaptive optics in giant telescopes," Advances in Adaptive Optics II. Proc. SPIE, 6272, 62723X (2006).
- [9] Saunter C. D. and Love, G. D., "Low cost, high speed control for adaptive optics," Proc. 6th International Workshop on Adaptive Optics for Industry and Medicine. (2007).
- [10] Wong, S., Vassiliadis, S., Cotofana, S., "A sum of absolute differences implementation in FPGA hardware," Euromicro Conference Proc. 28, 183 – 188 (2002).
- [11] J. Trujillo Sevil, M.R. Valido, L.F. Rodríguez Ramos, E. Boemo, F. Rosa, J.M. Rodríguez Ramos, "Real time phase-slopes calculations using FPGAs", Proceedings of SPIE, 7015.